

**Amendments to the Specification**

*Please replace the paragraph beginning at page 1, line 3, with the following:*

The present application is related to the following listed seven applications:

Serial No. [ ] 10/016,346, (now U.S. Patent No. 6,754,881) (~~RPS920010125US1~~)  
 entitled "Field Programmable Network Processor and Method for Customizing a Network  
 Processor;" Serial No. [ ] 10/016,772 (now U.S. Patent No. 6,806,730)  
 (~~RPS920010126US1~~), entitled "Method and System for Use of an Embedded Field Programmable  
 Gate Array Interconnect for Flexible I/O Connectivity;" Serial No. [ ] 10/016,449  
 (~~RPS920010127US1~~), entitled "Method and System for Use of a Field Programmable Gate Array  
 (FPGA) Function Within an Application Specific Integrated Circuit (ASIC) to Enable Creation of a  
 Debugger Client Within the ASIC;" Serial No. [ ] 10/016,448 (~~RPS 920010128US1~~),  
 entitled "Method and System for Use of a Field Programmable Function Within an Application  
 Specific Integrated Circuit (ASIC) To Access Internal Signals for External Observation and  
 Control;" Serial No. [ ] 10/015,922 (now U.S. Patent No. 6,593,771)  
 (~~RPS920010129US1~~), entitled "Method and System for Use of a Field Programmable Interconnect  
 Within an ASIC for Configuring the ASIC;" Serial No. [ ] 10/015,920 (now U.S.  
Patent No. 6,668,361) (~~RPS920010130US1~~), entitled "Method and System for Use of a Field  
 Programmable Function Within a Chip to Enable Configurable I/O Signal Timing Characteristics;  
 and " Serial No. [ ] 10/015,923 (now U.S. Patent No. 6,545,501) (~~RPS920010131US1~~),  
 entitled "Method and System for Use of a Field Programmable Function Within a Standard Cell  
 Chip for Repair of Logic Circuits;" assigned to the assignee of the present application, and filed on  
 the same date.